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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,448	12/10/2001	Robert Thomas Bailis	RPS920010128US1	5281

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/016,448	BAILIS ET AL.	
	Examin r	Art Unit	
	Cynthia Britt	2133	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Response to Amendment

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Specification

The disclosure is objected to because of the following informalities: The specification should be amended to include the patent numbers and/or the application numbers of copending applications.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. U.S. Patent No. 6,829,751.

As per claim 1, Shen et al. teaches providing a method and/or architecture for implementing a diagnostic architecture using an (*field programmable function*) FPGA core in a system on-chip design that can (i) ease bringing up, verification and debugging by providing interconnection and programming options; (ii) *observe* important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the *control* of the FPGA core; (iv) display appropriate signals on a debugging workstation, allowing many debugging features to be supported such as: (a) triggering and tracing based on *internal signals*, (b) dynamically changing host register values and (c) providing complex monitoring functions (*observation and control*), since the (*field programmable function*) FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market. (Column 1 line 56 through column 2 line12) The register block communicates with the FPGA core through a bus (*at least one bus coupled to at least a portion of the logic functions*). Similarly, the register block (*standard cell*) can also communicate with the FPGA core through other busses. The buses can be implemented as multi-bit buses or can also be implemented as single bit buses, if appropriate. Additionally, the buses can also be implemented as bidirectional buses. The FPGA core can also communicate with the control block (*standard cell*) through a bus. The FPGA core can communicate through a number of I/O pins over a bus. (Fig 2, column 3 lines 13-31) By using the FPGA core to implement such chip diagnostics, simultaneous probing of internal signals can be achieved while the system is running under predetermined conditions (e.g., a normal mode of operation). (Column 3 lines 32-42 figure 2) This circuit can also be implemented by the preparation of

(*application specific integrated circuit*) ASICS, FPGAs, or by interconnecting an appropriate network of conventional component circuits. (Column 5 lines 54-58) The circuit can provide a FPGA core in an ASIC architecture that eases chip bring up, verification and debugging by interconnection and programming options. This allows important signals of a chip to be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. This allow all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip. (Column 6 lines18-30)

As per claims 2 and 3, Shen et al. teaches one or more chip I/O pins are connected to the FPGA core. Such a connection can allow the FPGA core to monitor the I/O of the chip. In addition, one of the I/O pins can be connected as an input pin to the FPGA core. An internal module from the FPGA core can generate a signal to drive the chip during the chip debugging. With a system on chip design, the signals among different blocks can also be connected through the FPGA core. Additionally, the FPGA core can bridge signals between different modules. Such bridging can help in debugging of different modules, and can also help in isolating problems. (Fig 5 column 4 line 59 through column 5 line 4)

As per claims 4 and 5, Shen et al. teaches the FPGA core can simultaneously probe multiple internal signals. By utilizing the scan chain under the single step mode and with the on-chip FPGA core acting as the data process center (*providing external I/O in communication with first logic that selects internal signals*), all the signals on the chip can be observed. The FPGA core can be used to bridge the signals (*signal*

connector function) between different modules, and the under test mode, to isolate a specific module and drive signals to test the specific module. The FPGA core can also be used to add or verify bug fixes. (Column 6 lines 45-56, figures 2, 3, and 5)

As per claims 6–8, Shen et al. teaches the FPGA core can simultaneously probe multiple internal signals. By utilizing the scan chain under the single step mode and with the on-chip FPGA core acting as the data process center, all the signals on the chip can be observed. The FPGA core can be used to bridge the signals between different modules, and in the under test mode, to isolate a specific module and drive signals to test (*test program*) the specific module. The FPGA core can also be used to add or verify bug fixes (*error recovery and correction*). The process of the debugging workstation working with the on-chip FPGA core to generate debugging features can also be implemented. The system can provide functionality of CAD software that can be implemented to work with the diagnostics design (*error recovery and correction*). The system can allow for enhanced debugging capabilities (*error recovery and correction*) with the diagnostics design, such as searching for a specific signal pattern, tracing the internal state machine, and/or triggering on a programmed condition. The system can provide on the fly monitoring of the correctness of the bus protocol, doing statistics counting to measure the performance, and/or testing coverage. Column 6 lines 45-65

As per claim 9, Shen et al teaches providing a debugging workstation (*error written to external system*) (column 6 line 53-56).

As per claims 10 and 11, Shen et al. teaches the system can allow for enhanced debugging capabilities with the diagnostics design, such as searching for a specific

signal pattern, tracing the internal state machine and/or triggering on a programmed condition (*watchdog function, invoking error handling process*). As the system is programmable, it would be inherent that the system could be programmed to have a watchdog function (interval timer to detect possible malfunction – IEEE dictionary of standard terms) or other function for error handling. (Column 6 lines 57-65)

As per claim 12, Shen et al. teaches using a field programmable gate array core system. (Abstract Figure 1)

As per claim 13, Shen et al. teaches providing a method and/or architecture for implementing a diagnostic architecture using an (*field programmable function*) FPGA core in a system on-chip (*standard cell and logic functions*) design that can (i) ease bringing up, verification and debugging by providing interconnection and programming options; (ii) observe important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the *control* of the FPGA core; (iv) display appropriate signals on a debugging workstation (*observation*), allowing many debugging features to be supported such as: (a) triggering and tracing based on internal signals, (b) dynamically changing host register values and (c) providing complex monitoring functions (*observation and control*), since the FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market. (Column 1 line 56 through column 2 line12) This circuit can also be implemented by the preparation of (*application specific integrated circuit*) ASICS, FPGAs, or by interconnecting an appropriate network of conventional component circuits. (Column 5 lines 54-58) The circuit can provide a FPGA core in an ASIC architecture that eases chip bring up,

verification and debugging by interconnection and programming options (*test program*). This allows important signals of a chip to be observed while the chip is running under a normal mode by connecting the *internal signals* (*observation and control of internal signals*) to the FPGA core I/O. This allows all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip. (Column 6 lines18-30) By using the FPGA core to implement such chip diagnostics, simultaneous probing of internal signals can be achieved while the system is running under predetermined conditions (e.g., a normal mode of operation). (Column 3 lines 32-42 figure 2) The FPGA core can simultaneously probe multiple internal signals. By utilizing the scan chain under the single step mode and with the on-chip FPGA core acting as the data process center, all the signals on the chip can be observed. The FPGA core can be used to bridge the signals between different modules, and the under test mode, to isolate a specific module and drive signals to test (*test program*) the specific module. The FPGA core can also be used to add or verify bug fixes. Column 6 lines 45-65

As per claim 14, Shen et al. teaches an internal module from the FPGA core can generate a signal to drive the chip during the chip debugging. With a system on chip design, the signals among different blocks can also be connected through the FPGA core. Additionally, the FPGA core can bridge signals between different modules. Such bridging can help in debugging of different modules (validation of at least one module). Such bridging can also help in isolating problems. Column 6 lines 45-56

As per claim 15, Shen et al. teaches providing a method and/or architecture for implementing a diagnostic architecture using an FPGA core in a system on-chip (*standard cell, logic functions*) design that can (i) ease bringing up, verification and debugging by providing interconnection and programming options; (ii) observe important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the control of the FPGA core; (iv) display appropriate signals on a debugging workstation, allowing many debugging features to be supported such as: (a) triggering and tracing based on internal signals, (b) dynamically changing host register values and (c) providing complex monitoring functions (*test program*), since the FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market. (Column 1 line 56 through column 2 line12) This circuit can also be implemented by the preparation of (*application specific integrated circuit*) ASICS, FPGAs, or by interconnecting an appropriate network of conventional component circuits. (Column 5 lines 54-58) The circuit can provide a FPGA core in an ASIC architecture that eases chip bring up, verification and debugging by interconnection and programming options (*test program*). This allows important signals of a chip to be observed while the chip is running under a normal mode by connecting the *internal signals* (*observation and control of internal signals*) to the FPGA core I/O. This allows all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip. (Column 6 lines18-30) The FPGA core can simultaneously probe multiple *internal signals*. By utilizing the scan chain under the single step mode and with the on-chip FPGA core acting as the data process

center, all the signals on the chip can be observed. The FPGA core can be used to bridge the signals between different modules, and the under *test mode*, to isolate a specific module and drive signals to test the specific module. The FPGA core can also be used to add or verify bug fixes. (Column 6 lines 45-65)

As per claim 16, Shen et al. teaches that the FPGA core can simultaneously probe multiple internal signals. By utilizing the scan chain under the single step mode and with the on-chip FPGA core acting as the data process center, all the signals on the chip can be observed. The FPGA core can be used to bridge the signals between different modules, and the under test mode, to isolate a specific module and drive signals to test the specific module. The FPGA core can also be used to add or verify bug fixes (*determining if an error is observed and if observed, corrected*). The process of the debugging workstation working with the on-chip FPGA core to generate many powerful debugging features can also be implemented. (Column 6 lines 45-56)

As per claim 17, Shen et al. teaches providing a debugging workstation (*error written to external system*) (column 6 line 53-56).

As per claims 18 and 19, Shen et al. teaches the system can allow for enhanced debugging capabilities with the diagnostics design, such as searching for a specific signal pattern, tracing the internal state machine and/or triggering on a programmed condition (*watchdog function, invoking error handling process*). As the system is programmable, it would be inherent that the system could be programmed to have a watchdog function (interval timer to detect possible malfunction – IEEE dictionary of standard terms) or other function for error handling. (Column 6 lines 57-65)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,260,087 Chang

This patent teaches an Application Specific Integrated Circuit (ASIC), which includes at least one hardware, non-programmable functional block, also includes a programmable logic block (PLB). The PLB is electrically programmable for performing at least one function that complements a function performed using the hardware, non-programmable functional block. The presence of the PLB in the ASIC provides an opportunity to readily differentiate products within their respective product lines by adding particular functions to the ASIC, and to also functionally differentiate among various products offered by competing system builders.

U.S. Patent No. 6,211,697 Lien et al.

This patent teaches an integrated circuit (IC) including both a field-programmable gate array (FPGA) and a hard array (HA). The FPGA includes a first set of functional groups that each include an underlying logic structure and memory cells for programming the underlying logic structure, a first set of routing buses, and a first set of routing interconnect areas that provide interconnections between the first set of functional groups and the first set of routing buses. The first set of routing interconnect areas

includes transistors and memory cells for programming the interconnections. The HA includes a second set of functional groups that is equal in number to the first set of functional groups and that are arranged like the first set of functional groups. Each functional group in the second set of functional groups includes an underlying logic structure that is like the underlying logic structure of the first set of functional groups but which does not include memory cells for programming the underlying logic structure. The HA also includes a second set of routing buses that are arranged like the first set of routing buses and a second set of routing interconnect areas that are arranged like the first set of routing interconnect areas but which do not include transistors and memory cells for programming interconnections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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